CLAIMS

What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. Ramp generating circuitry comprising:

an array of capacitances, each with a first lead connected to provide a combined output voltage and a second lead; and

voltage control circuitry connected to the second lead of each of a set of two or more capacitances in said array, said voltage control circuitry controlling a voltage on each of said set of capacitances to produce a ramp signal of said combined output voltage.

2. The ramp generating circuitry according to claim 1, in which the voltage control circuitry includes a multi-bit shift register with an output for each bit that controls whether said one of said respective low voltage and said high voltage is provided to a capacitance in said set.

3. The ramp generating circuitry according to claim 1, in which said set of capacitances includes all capacitances in said array.

4. A ramp generator comprising:

a multi-bit shift register with a clock signal input, a reset signal input and, for each bit, an output;

clock signal circuitry that provides a clock signal to said shift register's clock signal input;

reset signal circuitry that provides a reset signal to said shift register's reset signal input;

an array of capacitors having a common top plate and each of said array of capacitors having a bottom plate switched sequentially to one of a low reference voltage and a high reference voltage in response to a respective shift register bit's output, a charge

on each of said capacitors in said array added to a ramp output signal on said top plate in response to a value in said shift register.

5. The ramp generator according to claim 4, further comprising a clamp-up switch and a clamp-down switch to terminate said ramp output signal.

6. The ramp generator according to claim 4, wherein said ramp output signal from said ramp generator is non-buffered.

7. The ramp generator according to claim 4, wherein said ramp output signal from said ramp generator is buffered.

8. The ramp generator according to claim 4, wherein said capacitors of said array are all the same size.

9. The ramp generator according to claim 4, wherein said capacitors of said array vary in size.

10. The ramp generator according to claim 9, wherein said capacitors of said array increase in size.

11. The ramp generator according to claim 10, wherein said increase in size produces a non-linear ramp for signal compression.

12. The ramp generator according to claim 9, wherein said capacitors of said array decrease in size.

13. A ramp analog-to-digital (ADC) converter comprising:

a ramp generator that includes:

an array of capacitances, each with a first lead connected to provide a combined output voltage and a second lead;

voltage control circuitry connected to the second lead of each of a set of two or more capacitances in said array, said voltage control circuitry controlling a voltage on each of said set of capacitances to produce a ramp signal of said combined output voltage; and

ADC comparison circuitry that receives an analog input signal and said ramp signal of said combined output voltage, said ADC comparison circuitry providing a digital output signal indicating magnitude of said analog input signal.

14. A ramp analog-to-digital converter (ADC) comprising:

an amplifier for receiving an analog voltage signal from a pixel;

a sample-and hold switch coupled to said amplifier;

a first comparator coupled to said sample-and-hold switch;

a second comparator coupled to said first comparator;

a synchronization latch coupled to said second comparator;

a counter coupled to said synchronization latch; and

ramp generation circuitry comprising:

an array of capacitances, each with a first lead connected to provide a combined output voltage and a second lead; and

voltage control circuitry connected to the second lead of each of a set of two or more capacitances in said array, said voltage control circuitry controlling a voltage on each of said set of capacitances to produce a ramp signal of said combined output voltage.

15. A ramp analog-to-digital converter (ADC) comprising:

an amplifier for receiving an analog voltage signal from a pixel;

a sample-and hold switch coupled to said amplifier;

a first comparator coupled to said sample-and-hold switch;

a second comparator coupled to said first comparator;

a synchronization latch coupled to said second comparator;

a counter coupled to said synchronization latch; and

a ramp generator comprising:

a multi-bit shift register with a clock signal input, a reset signal input and for each bit an output;

clock signal circuitry that provides a clock signal to said shift register's clock signal input;

reset signal circuitry that provides a reset signal to said shift register's reset signal input; and

an array of capacitors having a common top plate and each of said array of capacitors having a bottom plate switched sequentially to one of a low reference voltage and a high reference voltage in response to a respective shift register bit's output, a charge on each of said capacitors in said array added to a ramp output signal on said top plate in response to a value in said shift register.

16. The ramp ADC according to claim 15, wherein said first comparator further comprises a reset switch and a capacitor.

17. The ramp ADC according to claim 15, wherein said second comparator further comprises a reset switch and a capacitor.

18. A ramp analog-to-digital converter (ADC) comprising:

an amplifier for receiving an analog voltage signal from a pixel;

a sample-and hold switch coupled to said amplifier;

a comparator coupled to said sample-and-hold switch;

a synchronization latch coupled to said comparator;

a logic gate coupled to said synchronization latch;

a counter coupled to said logic gate; and

a ramp generator comprising:

an array of capacitances, each with a first lead connected to provide a combined output voltage and a second lead; and

voltage control circuitry connected to the second lead of each of a set of two or more capacitances in said array, said voltage control circuitry controlling a voltage on each of said set of capacitances to produce a ramp signal of said combined output voltage.

19. A ramp analog-to-digital converter (ADC) comprising:

an amplifier for receiving an analog voltage signal from a pixel;

a sample-and hold switch coupled to said amplifier;

a comparator coupled to said sample-and-hold switch;

a synchronization latch coupled to said comparator;

a logic gate coupled to said synchronization latch;

a counter coupled to said logic gate; and

a ramp generator comprising:

a multi-bit shift register with a clock signal input, a reset signal input and for each bit an output;

clock signal circuitry that provides a clock signal to said shift register's clock signal input;

reset signal circuitry that provides a reset signal to said shift register's reset signal input; and

an array of capacitors having a common top plate and each of said array of capacitors having a bottom plate switched sequentially to one of a low reference voltage and a high reference voltage in response to a respective shift register bit's output, a charge on each of said capacitors in said array added to a ramp output signal on said top plate in response to a value in said shift register.

20. An imaging device comprising:

an amplifier for receiving an analog voltage signal from a pixel;

a sample-and-hold switch coupled to said amplifier;

a first comparator coupled to said sample-and-hold switch;

a second comparator coupled to said first comparator;

a synchronization latch coupled to said second comparator;

a counter coupled to said synchronization latch; and

a ramp generator comprising:

a multi-bit shift register with a clock signal input, a reset signal input and for each bit an output;

clock signal circuitry that provides a clock signal to said shift register's clock signal input;

reset signal circuitry that provides a reset signal to said shift register's reset signal input; and

an array of capacitors having a common top plate and each of said array of capacitors having a bottom plate switched sequentially to one of a low reference voltage and a high reference voltage in response to a respective shift register bit's output, a charge on each of said capacitors in said array added to a ramp output signal on said top plate in response to a value in said shift register.

21. An imaging device comprising:

an array of pixels;

a signal processing circuit that receives analog signals from pixels in said pixel array and provides, for each analog signal, a corresponding digital signal; and

ramp generating circuitry that provides a ramp signal to said signal processing circuitry, said ramp generating circuitry including:

an array of capacitances, each with a first lead connected to provide a combined output voltage and a second lead; and

voltage control circuitry connected to the second lead of each of a set of two or more capacitances in said array, said voltage control circuitry controlling a voltage on each of said set of capacitances to produce a ramp signal of said combined output voltage.

22. The imaging device according to claim 21, wherein there is a single ramp generating circuit.

23. The imaging device according to claim 21, wherein there are at least two ramp generating circuits.

24. The imaging device according to claim 21, wherein said array of pixels includes columns of pixels and said signal processing circuit includes an array of column processing circuits.

25. The imaging device according to claim 24 wherein each column processing circuit includes an analog-to-digital circuit that receives ramp signals from said ramp generating circuitry.

26. The imaging device according to claim 21, wherein said signal processing circuitry includes an analog-to-digital converter (ADC).

27. The imaging device according to claim 26, wherein said array of pixels includes columns of pixels and further comprising multiplexing circuitry for providing analog pixel signals for each column to said analog-to-digital circuit.

28. An imaging device comprising:

an array of pixels;

a signal processing circuit that receives analog signals from pixels in said pixel array and provides for each analog signal a corresponding digital signal; and

ramp generating circuitry that provides a ramp signal to said signal processing circuitry, said ramp generating circuitry including:

a multi-bit shift register with a clock signal input, a reset signal input and, for each bit, an output;

clock signal circuitry that provides a clock signal to said shift register's clock signal input;

reset signal circuitry that provides a reset signal to said shift register's reset signal input;

an array of capacitors having a common top plate and each of said array of capacitors having a bottom plate switched sequentially to one of a low reference voltage

and a high reference voltage in response to a respective shift register bit's output, a charge on each of said capacitors in said array added to a ramp output signal on said top plate in response to a value in said shift register.

29. The imaging device according to claim 28, wherein said array of pixels includes columns of pixels and said signal processing circuit includes, for each column, an analog-to-digital circuit the receives said ramp signal from said ramp generating circuitry.

30. An imaging device comprising:

an amplifier for receiving an analog voltage signal from a pixel;

a sample-and hold switch coupled to said amplifier;

a comparator coupled to said sample-and-hold switch;

a synchronization latch coupled to said comparator;

a logic gate coupled to said synchronization latch;

a counter coupled to said logic gate; and

a ramp generator comprising:

a multi-bit shift register with a clock signal input, a reset signal input and for each bit an output;

clock signal circuitry that provides a clock signal to said shift register's clock signal input;

reset signal circuitry that provides a reset signal to said shift register's reset signal input; and

an array of capacitors having a common top plate and each of said array of capacitors having a bottom plate switched sequentially to one of a low reference voltage and a high reference voltage in response to a respective shift register bit's output, a charge on each of said capacitors in said array added to a ramp output signal on said top plate in response to a value in said shift register.

31. An imaging device comprising:

an amplifier for receiving an analog voltage signal from a pixel;

a sample-and-hold switch coupled to said amplifier;

a first comparator coupled to said sample-and-hold switch;

a second comparator coupled to said first comparator;

a synchronization latch coupled to said second comparator;

a counter coupled to said synchronization latch; and

a ramp generator comprising:

an array of capacitances, each with a first lead connected to provide a combined output voltage and a second lead; and

voltage control circuitry connected to the second lead of each of a set of two or more capacitances in said array, said voltage control circuitry controlling a voltage on each of said set of capacitances to produce a ramp signal of said combined output voltage.

32. An imaging device comprising:

an amplifier for receiving an analog voltage signal from a pixel;

a sample-and hold switch coupled to said amplifier;

a comparator coupled to said sample-and-hold switch;

a synchronization latch coupled to said comparator;

a logic gate coupled to said synchronization latch;

a counter coupled to said logic gate; and

a ramp generator comprising:

an array of capacitances, each with a first lead connected to provide a combined output voltage and a second lead; and

voltage control circuitry connected to the second lead of each of a set of two or more capacitances in said array, said voltage control circuitry controlling a voltage on each of said set of capacitances to produce a ramp signal of said combined output voltage.

33. An integrated circuit comprising:

an array of pixel cells for sensing images, the array including two or more readout lines, each readout line being connected to a respective set of said pixel cells; and

readout circuitry outside the array of pixel cells, said readout circuitry including, for each readout line, a ramp analog-to-digital converter (ADC), that includes:

a ramp generator that includes:

an array of capacitances, each with a first lead connected to provide a combined output voltage and a second lead;

voltage control circuitry connected to the second lead of each of a set of two or more capacitances in said array, said voltage control circuitry controlling a voltage on each of said set of capacitances to produce a ramp signal of said combined output voltage; and

ADC comparison circuitry that receives an analog input signal and said ramp signal of said combined output voltage, said ADC comparison circuitry providing a digital output signal indicating magnitude of said analog input signal.

34. The integrated circuit according to claim 33, in which the array of pixel cells includes rows and columns of pixel cells, each readout line being connected to said pixel cells in a respective column.

35. An imaging system comprising:

a processor;

a memory device coupled to said processor via a bus; and

an imaging device, said imaging device comprising:

an amplifier for receiving an analog voltage signal from a pixel;

a sample-and-hold switch coupled to said amplifier;

a first comparator coupled to said sample-and-hold switch;

a second comparator coupled to said first comparator;

a synchronization latch coupled to said second comparator;

a counter coupled to said synchronization latch; and

a ramp generator comprising:

an array of capacitances, each with a first lead connected to provide a combined output voltage and a second lead; and

voltage control circuitry connected to the second lead of each of a set of two or more capacitances in said array, said voltage control circuitry controlling a voltage on each of said set of capacitances to produce a ramp signal of said combined output voltage.

36. An imaging system comprising:

a processor;

a memory device coupled to said processor via a bus; and

an imaging device, said imaging device comprising:

an amplifier for receiving an analog voltage signal from a pixel;

a sample-and-hold switch coupled to said amplifier;

a first comparator coupled to said sample-and-hold switch;

a second comparator coupled to said first comparator;

a synchronization latch coupled to said second comparator;

a counter coupled to said synchronization latch; and

a ramp generator comprising:

a multi-bit shift register with a clock signal input, a reset signal input and for each bit an output;

clock signal circuitry that provides a clock signal to said shift register's clock signal input;

reset signal circuitry that provides a reset signal to said shift register's reset signal input; and

an array of capacitors having a common top plate and each of said array of capacitors having a bottom plate switched sequentially to one of a low reference voltage and a high reference voltage in response to a respective shift register bit's output, a charge on each of said capacitors in said array added to a ramp output signal on said top plate in response to a value in said shift register.

37. An imaging system comprising:

a processor;

a memory device coupled to said processor via a bus; and

an imaging device, said imaging device comprising:

an amplifier for receiving an analog voltage signal from a pixel;

a sample-and hold switch coupled to said amplifier;

a comparator coupled to said sample-and-hold switch;

a synchronization latch coupled to said comparator;

a logic gate coupled to said synchronization latch;

a counter coupled to said logic gate; and

a ramp generator comprising:

an array of capacitances, each with a first lead connected to provide a combined output voltage and a second lead; and

voltage control circuitry connected to the second lead of each of a set of two or more capacitances in said array, said voltage control circuitry controlling a voltage on each of said set of capacitances to produce a ramp signal of said combined output voltage.

38. An imaging system comprising:

a processor;

a memory device coupled to said processor via a bus; and

an imaging device, said imaging device comprising:

an amplifier for receiving an analog voltage signal from a pixel;

a sample-and hold switch coupled to said amplifier;

a comparator coupled to said sample-and-hold switch;

a synchronization latch coupled to said comparator;

a logic gate coupled to said synchronization latch;

a counter coupled to said logic gate; and

a ramp generator comprising:

a multi-bit shift register with a clock signal input, a reset signal input and for each bit an output;

clock signal circuitry that provides a clock signal to said shift register's clock signal input;

reset signal circuitry that provides a reset signal to said shift register's reset signal input; and

an array of capacitors having a common top plate and each of said array of capacitors having a bottom plate switched sequentially to one of a low reference voltage and a high reference voltage in response to a respective shift register bit's output, a charge on each of said capacitors in said array added to a ramp output signal on said top plate in response to a value in said shift register.

39. A ramp generator comprising:

a multi-bit shift register with a clock signal input, a reset signal input and for each bit an output;

clock signal circuitry that provides a clock signal to said shift register's clock signal input;

reset signal circuitry that provides a reset signal to said shift register's reset signal input;

first and second paired common plate lines;

an array of capacitor circuits, each capacitor circuit including:

a first capacitor connected between a switchable high voltage source and said first common plate;

a second capacitor connected between a switchable low voltage source and said second common plate; and

a switch connected between said first capacitor's connection to said high voltage source and said second capacitor's connection to said low voltage source; and

a reference voltage signal switchably coupled to said first common plate and said second common plate.

40. The ramp generator according to claim 39, wherein each capacitor of each capacitor circuit is the same size.

41. The ramp generator according to claim 39, wherein each capacitor of each capacitor circuit can vary in size.

42. The ramp generator according to claim 41, wherein each capacitor of each capacitor circuit increases in size across said array of capacitor circuits.

43. The ramp generator according to claim 42, wherein said increase in size produces a non-linear ramp for signal compression.

44. The ramp generator according to claim 39, wherein each capacitor of each capacitor circuit decreases in size across said array of capacitor circuits.

45. A ramp analog-to-digital converter (ADC) comprising:

an amplifier for receiving an analog voltage signal from a pixel;

a sample-and hold switch coupled to said amplifier;

a first comparator coupled to said sample-and-hold switch;

a second comparator coupled to said first comparator;

a synchronization latch coupled to said second comparator;

a counter coupled to said synchronization latch; and

a ramp generator comprising:

a multi-bit shift register with a clock signal input, a reset signal input and for each bit an output;

clock signal circuitry that provides a clock signal to said shift register's clock signal input;

reset signal circuitry that provides a reset signal to said shift register's reset signal input;

first and second paired common plate lines;

an array of capacitor circuits, each capacitor circuit including:

a first capacitor connected between a switchable high voltage source and said first common plate;

a second capacitor connected between a switchable low voltage source and said second common plate; and

a switch connected between said first capacitor's connection to said high voltage source and said second capacitor's connection to said low voltage source; and

a reference voltage signal switchably coupled to said first common plate and said second common plate.

46. The ramp ADC according to claim 45, wherein said first comparator further comprises a first reset switch, a second reset switch, a first capacitor and a second capacitor.

47. The ramp ADC according to claim 45, wherein said second comparator further comprises a first reset switch, a second reset switch, a first capacitor and a second capacitor.

48. An imaging device comprising:

an amplifier for receiving an analog voltage signal from a pixel;

a sample-and-hold switch coupled to said amplifier;

a first comparator coupled to said sample-and-hold switch;

a second comparator coupled to said first comparator;

a synchronization latch coupled to said second comparator;

a counter coupled to said synchronization latch; and

a ramp generator comprising:

a multi-bit shift register with a clock signal input, a reset signal input and for each bit an output;

clock signal circuitry that provides a clock signal to said shift register's clock signal input;

reset signal circuitry that provides a reset signal to said shift register's reset signal input;

first and second paired common plate lines;

an array of capacitor circuits, each capacitor circuit including:

a first capacitor connected between a switchable high voltage source and said first common plate;

a second capacitor connected between a switchable low voltage source and said second common plate; and

a switch connected between said first capacitor's connection to said high voltage source and said second capacitor's connection to said low voltage source; and

a reference voltage signal switchably coupled to said first common plate and said second common plate.

49. An imaging system comprising:

a processor;

a memory device coupled to said processor via a bus; and

an imaging device, said imaging device comprising:

an amplifier for receiving an analog voltage signal from a pixel;

a sample-and-hold switch coupled to said amplifier;

a first comparator coupled to said sample-and-hold switch;

a second comparator coupled to said first comparator;

a synchronization latch coupled to said second comparator;

a counter coupled to said synchronization latch; and

a ramp generator comprising:

a multi-bit shift register with a clock signal input, a reset signal input and for each bit an output;

clock signal circuitry that provides a clock signal to said shift register's clock signal input;

reset signal circuitry that provides a reset signal to said shift register's reset signal input;

first and second paired common plate lines;

an array of capacitor circuits, each capacitor circuit including:

a first capacitor connected between a switchable high voltage source and said first common plate;

a second capacitor connected between a switchable low voltage source and said second common plate; and

a switch connected between said first capacitor's connection to said high voltage source and said second capacitor's connection to said low voltage source; and

a reference voltage signal switchably coupled to said first common plate and said second common plate.

50. A method of operating a ramp generator comprising:

applying a clock signal to a shift register, wherein each time said clock signal is applied to said shift register a count in said shift register is incremented; and

sequentially switching from a low reference voltage to a high reference voltage via a plurality of capacitors arranged in an array, a charge on each of said plurality of capacitors added to an output of said ramp generator in response to said count in said shift register.

51. The method according to claim 50, further comprising applying a reset signal to said shift register.

52. A method of operating a ramp analog-to-digital converter (ADC) comprising:

resetting a pixel via a pixel reset signal;

releasing said pixel reset signal;

resetting an amplifier via an amplifier reset signal;

concurrently resetting a first comparator via a first comparator reset signal and a second comparator via a second comparator reset signal;

releasing said amplifier reset signal;

releasing said first comparator reset signal;

releasing said second comparator reset signal;

dumping a photogate charge onto a pixel sensing node;

amplifying said photogate charge;

storing said amplified photogate charge in a sample-and hold circuit; and

applying a ramp voltage signal generated by a ramp generator to compensate the amplified photogate signal.

53. A method of generating a ramp signal comprising:

during each interval of a series of intervals, providing to an input lead of each of a set of capacitances, one of a respective low voltage and a respective high voltage, said capacitances having output leads that are connected to provide a combined output voltage; and

providing, in each interval, said one of said respective low voltage and said respective high voltage to produce said ramp signal, said ramp signal being said combined output voltage over said series of intervals.

54. A method of operating an integrated circuit comprising:

resetting a pixel via a pixel reset signal;

releasing said pixel reset signal;

resetting an amplifier via an amplifier reset signal;

concurrently resetting a first comparator via a first comparator reset signal and a second comparator via a second comparator reset signal;

releasing said amplifier reset signal;

releasing said first comparator reset signal;

releasing said second comparator reset signal;

dumping a photogate charge onto a pixel sensing node;

amplifying said photogate charge;

storing said amplified photogate charge in a sample-and hold circuit; and

applying a ramp voltage signal generated by a ramp generator to compensate the amplified photogate signal.

55. A method of operating an imaging device comprising:

resetting a pixel via a pixel reset signal;

releasing said pixel reset signal;

resetting an amplifier via an amplifier reset signal;

concurrently resetting a first comparator via a first comparator reset signal and a second comparator via a second comparator reset signal;

releasing said amplifier reset signal;

releasing said first comparator reset signal;

releasing said second comparator reset signal;

dumping a photogate charge onto a pixel sensing node;

amplifying said photogate charge;

storing said amplified photogate charge in a sample-and hold circuit; and

applying a ramp voltage signal generated by a ramp generator to compensate the amplified photogate signal.

56. A method of operating an imaging system comprising:

resetting a pixel via a pixel reset signal;

releasing said pixel reset signal;

resetting an amplifier via an amplifier reset signal;

concurrently resetting a first comparator via a first comparator reset signal and a second comparator via a second comparator reset signal;

releasing said amplifier reset signal;

releasing said first comparator reset signal;

releasing said second comparator reset signal;

dumping a photogate charge onto a pixel sensing node;

amplifying said photogate charge;

storing said amplified photogate charge in a sample-and hold circuit; and

applying a ramp voltage signal generated by a ramp generator to compensate the amplified photogate signal.

57. An integrated circuit comprising:

ramp generating circuitry, said ramp generating circuitry further comprising:

an array of capacitances, each with a first lead connected to provide a combined output voltage and a second lead; and

voltage control circuitry that provides to said second lead, a set of capacitances, one of a respective low voltage and a high voltage during each of a series of intervals, said voltage control circuitry providing said one of said respective low voltage and said high voltage in each interval to produce a ramp of said combined output voltage over said series of intervals.

58. An imaging device comprising:

a pixel array; and

an array of analog-to-digital converters (ADCs), each ADC of said array of ADCs further comprising:

an amplifier for receiving an analog voltage signal from a pixel of said pixel array;

a sample-and-hold switch coupled to said amplifier;

a first comparator coupled to said sample-and-hold switch;

a second comparator coupled to said first comparator;

a synchronization latch coupled to said second comparator;

a counter coupled to said synchronization latch; and

ramp generating circuitry further comprising:

an array of capacitances, each with a first lead connected to provide a combined output voltage and a second lead; and

voltage control circuitry connected to the second lead of each of a set of two or more capacitances in said array, said voltage control circuitry controlling a voltage on each of said set of capacitances to produce a ramp signal of said combined output voltage.

59. An imaging device comprising:

a pixel array; and

an array of analog-to-digital converters (ADCs), each ADC of said array of ADCs further comprising:

an amplifier for receiving an analog voltage signal from a pixel;

a sample-and hold switch coupled to said amplifier;

a comparator coupled to said sample-and-hold switch;

a synchronization latch coupled to said comparator;

a logic gate coupled to said synchronization latch;

a counter coupled to said logic gate; and

ramp generating circuitry further comprising:

an array of capacitances, each with a first lead connected to provide a combined output voltage and a second lead; and

voltage control circuitry connected to the second lead of each of a set of two or more capacitances in said array, said voltage control circuitry controlling a voltage on each of said set of capacitances to produce a ramp signal of said combined output voltage.

60. Ramp generating circuitry comprising:

an array of capacitances, each with a first lead connected to provide a combined output voltage and a second lead; and

voltage control circuitry that provides to said second lead of a set of capacitances in the array one of a respective low voltage and a high voltage during each of a series of intervals, said voltage control circuitry providing said one of said respective low voltage and said high voltage in each interval to produce a ramp of said combined output voltage over said series of intervals.